ABSTRACT OF THE DISCLOSURE

Above a memory block including horizontal memory cells in 8 rows by 256 columns, a total of eight lines, a global word line, a bit line load power supply line, a local data input/output line pair, a bit line signal input/output line pair, a memory cell power supply line and a global column selecting line are arranged at equal intervals. Since provision of one line is enough per one memory cell row, an SRAM having a T-type bit line structure can be realized with ease using horizontal memory cells to enable reduction of a layout area and speed-up of an operation rate.